

ELEN E3106/4106 Lecture 20

MOS Capacitor Part II Outline

- PMOS vs NMOS
- PMOS band diagrams under biasing conditions
- C-V characteristics
- Non-idealities in the C-V curves
- CCD imager applications

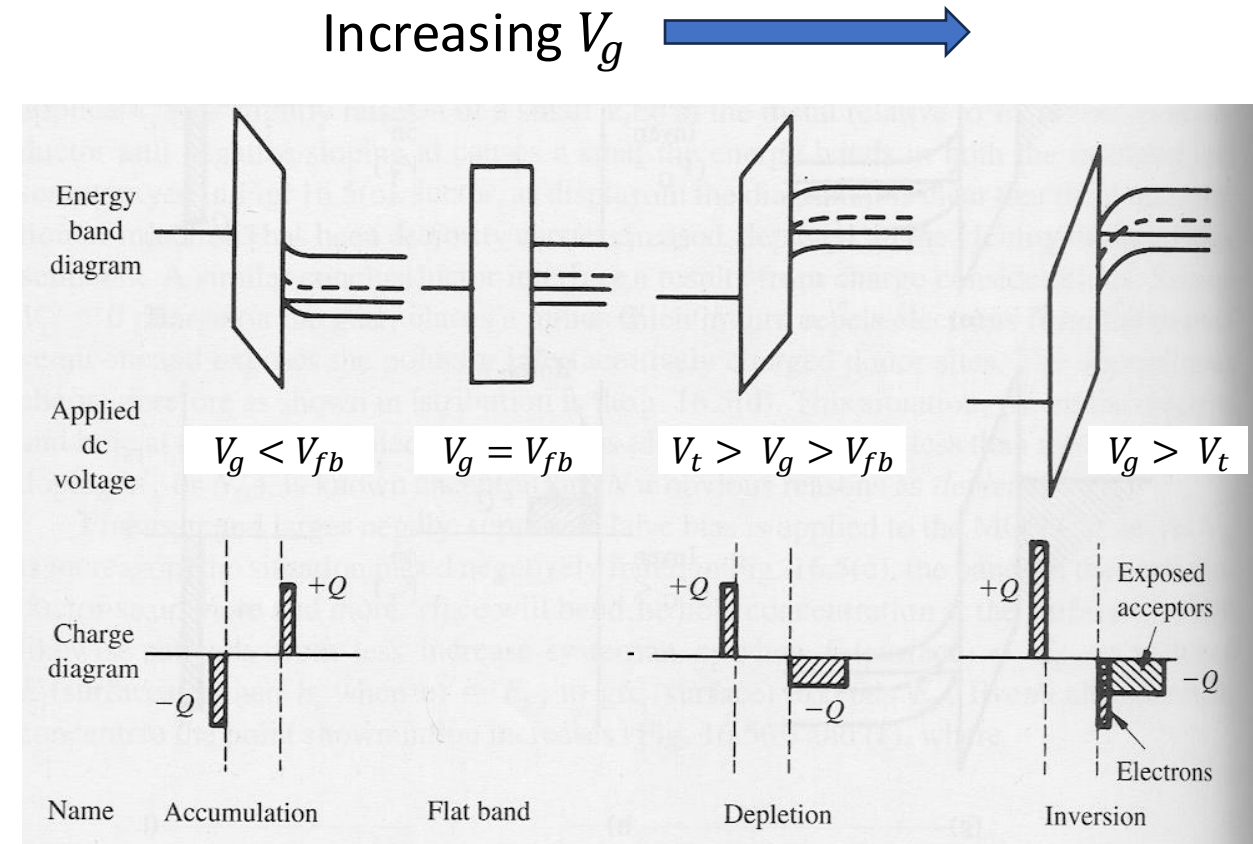
Assignments:

Reading: C. Hu §5.6, 5.10.1

Homework 8 due Monday Dec. 1st by 11:59pm

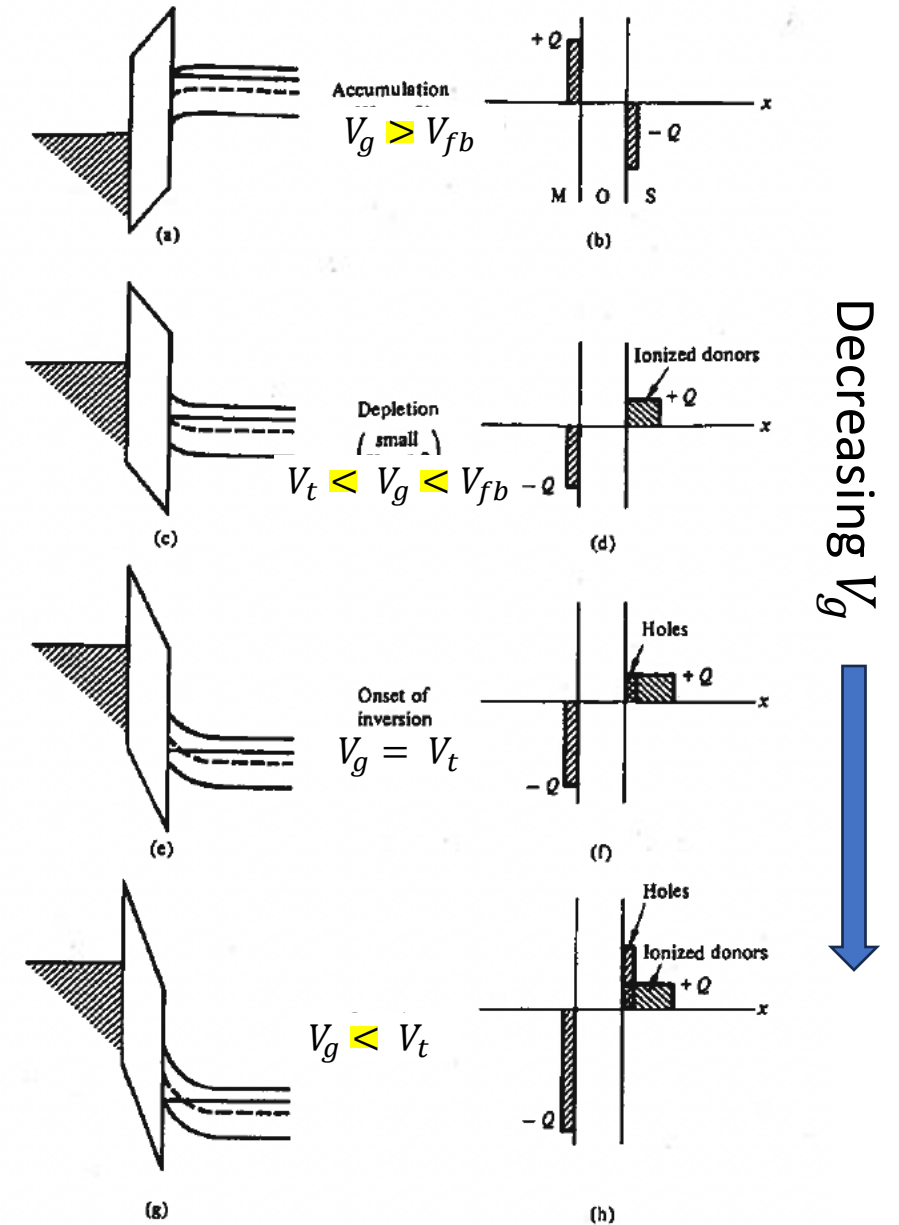
Recap of MOS Capacitors So Far...

- We discussed different gate bias conditions
 - Accumulation
 - Flat-band
 - Depletion
 - Threshold
 - Inversion
- Note we have focused on NMOS (the inversion layer is made of)
- Recall: y-axis of band diagram represents energy of an e-
- Voltage corresponds to P.E. of *positive* charge, so reduces energy of e- and bends the bands
- Assumption: No charge inside of oxide!



PMOS Capacitor

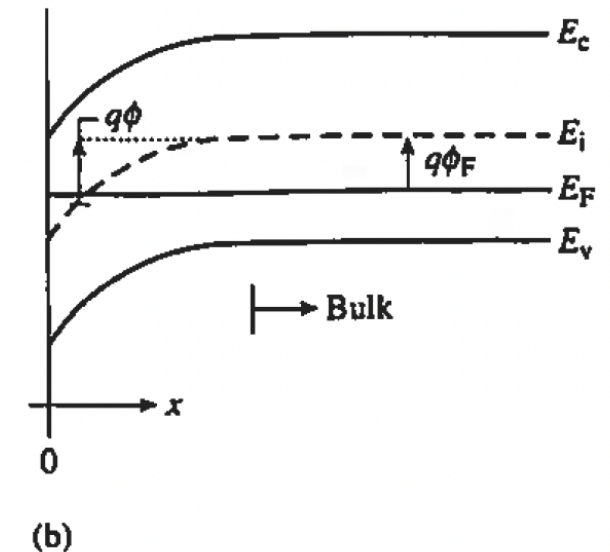
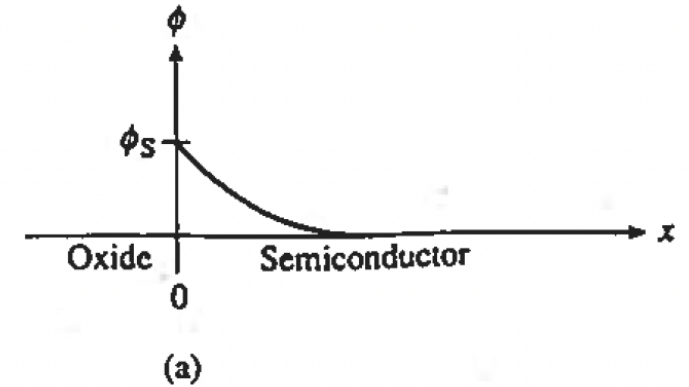
- *n*-type semiconductor body with _____ inversion layer of holes at the _____
- Same gate bias conditions, but the sign on the gate is flipped
 - Accumulation: e- accumulate at surface
 - Flat-band: no E-field
 - Depletion: e- repelled from surface
 - Threshold: onset of inversion ($p_s = \text{_____}$)
 - Inversion: surface becomes p-type



Another look at Surface and Bulk Potential

- Let $\Phi(x)$ be the electrostatic potential inside the semiconductor at any point ____
 - $\Phi(x) = \frac{1}{q} [E_i(bulk) - E_i(x)]$
- Let $x = \underline{\hspace{1cm}}$ at the oxide-metal interface. The surface potential is:
 - $\Phi_s = \Phi(x = 0) = \frac{1}{q} [E_i(bulk) - E_i(surface)]$
- As x increases, the E-field goes to ____
- But what about Φ_F ? Recall $\Phi_s = \underline{\hspace{1cm}}$ at the depletion-inversion threshold
 - $\Phi_F = \frac{1}{q} [E_i(bulk) - E_F]$
 - This is a material parameter! Since it depends on E_F , it depends on the ____
 - For p-type bulk (NMOS): $\Phi_F = \frac{kT}{q} \ln \left(\frac{N_a}{n_i} \right) > 0$
 - For n-type bulk (PMOS): $\Phi_F = \frac{kT}{q} \ln \left(\frac{N_d}{n_i} \right) < 0$

Graphical definition of $\Phi(x)$, $\Phi_s(a)$. The relationship between $\Phi(x)$ and bending bending; graphical definition of $\Phi_F(b)$.



- Why do we denote these potentials Φ instead of V?

Weak vs. Strong Inversion in MOS caps

Weak Inversion

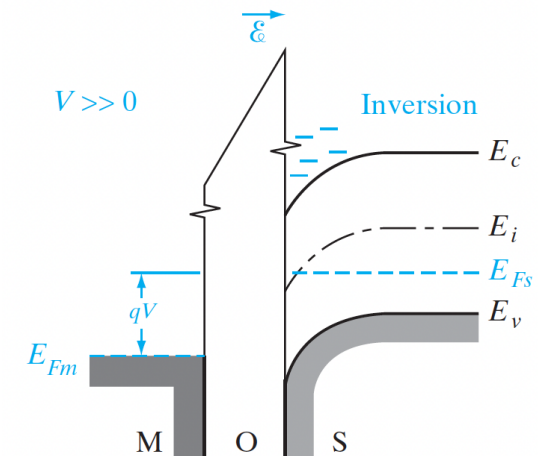
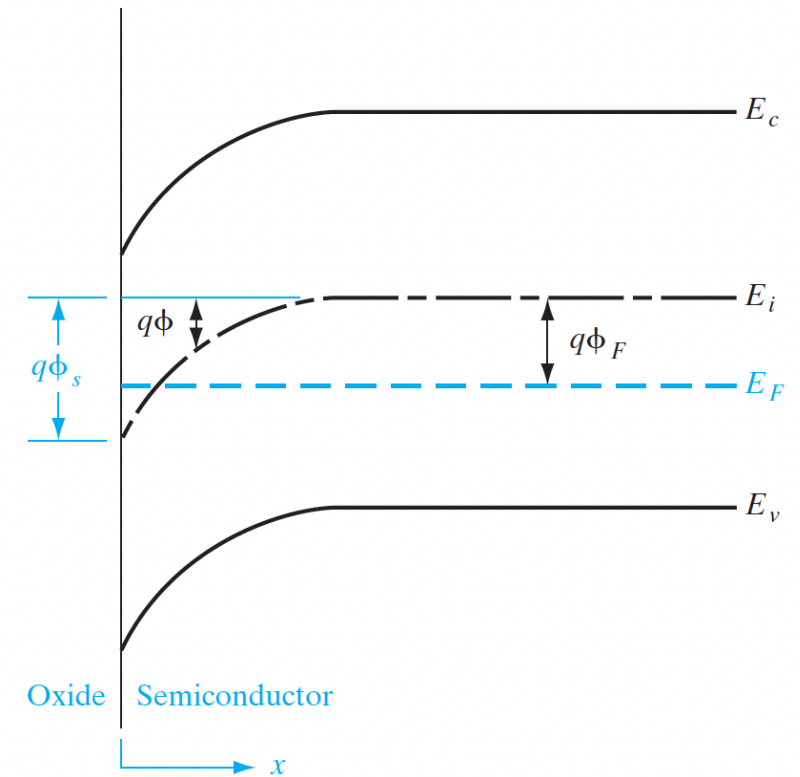
- Occurs when $\Phi_F < \Phi_S < 2 \Phi_F$
- The intrinsic level E_i at the surface has just crossed below the Fermi level E_F
- The surface is inverted in type (e.g., p-type substrate becomes weakly n-type), but the **inversion charge** is still small compared to the **depletion charge**!

Strong Inversion: $\phi_s(\text{inv.}) = 2\phi_F = 2 \frac{kT}{q} \ln \frac{N_a}{n_i}$

- Condition: The surface is **as strongly inverted** as the bulk is doped:

$n_{\text{surface}} = p_{\text{bulk}}$ (surface electron density equals bulk hole density).

- The intrinsic level E_i at the surface lies as far **below** E_F



Energy Band Diagram Summary

- Energy band diagrams for the two dominant types of MOS caps shown here

- _____ (NMOS) devices have an _____ inversion layer. The bulk is p-type.

- $p_{bulk} \approx N_a$

- _____ (PMOS) devices have a _____ inversion layer. The bulk is n-type.

- $n_{bulk} \approx N_d$

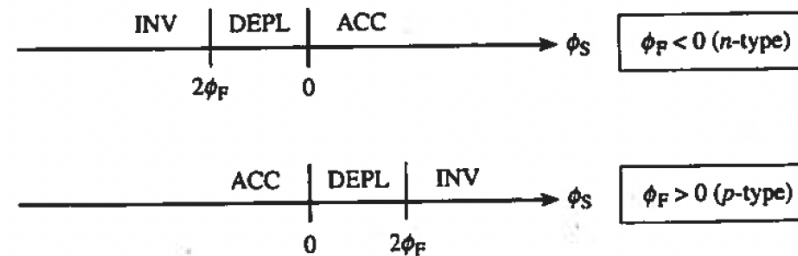
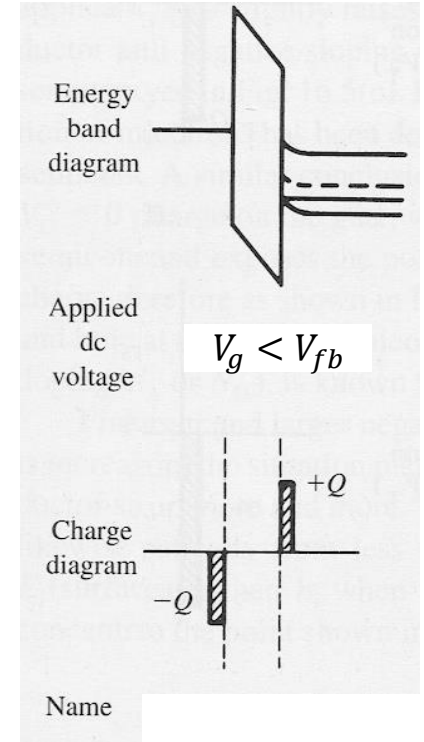


FIGURE 5-33 Energy band diagrams of the two dominant types of MOS capacitors. An N-type device is so named because it has N-type inversion charge that increases with a more positive V_g , and a P-type device has P-type inversion charge increasing with a more negative V_g .

Guidelines for Drawing MOS Band Diagrams

- E_F is flat (constant with distance x) in the semiconductor
-
- Since no current flows, we assume _____ conditions hold
 - Band bending is linear in the oxide ($\frac{dE_c}{dx}$ is const.)
 - No charge in oxide ($\frac{dE}{dx} = 0$) so E-field is constant
 - The MOS “type” refers to the type of _____ layer
 - As we’ve seen with every other device type, there’s an equivalent p-type MOS cap to an n-type MOS cap
 - p⁺-poly gate over n-type substrate
 - The vertical distance between the Fermi level in the metal and the Fermi level in the Si body is equal to the applied gate voltage: $qV_g = E_{F,semi} - E_{F,m}$



Problem: Calculating Flat-band and Threshold Voltages

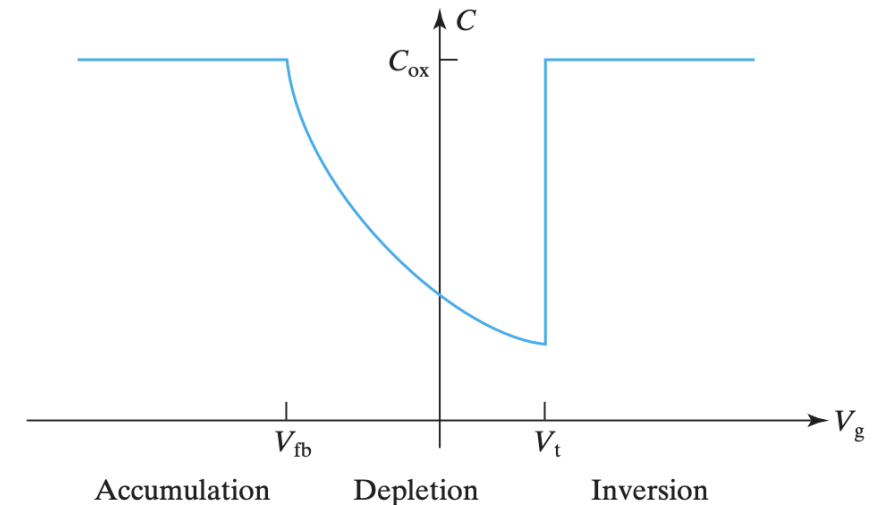
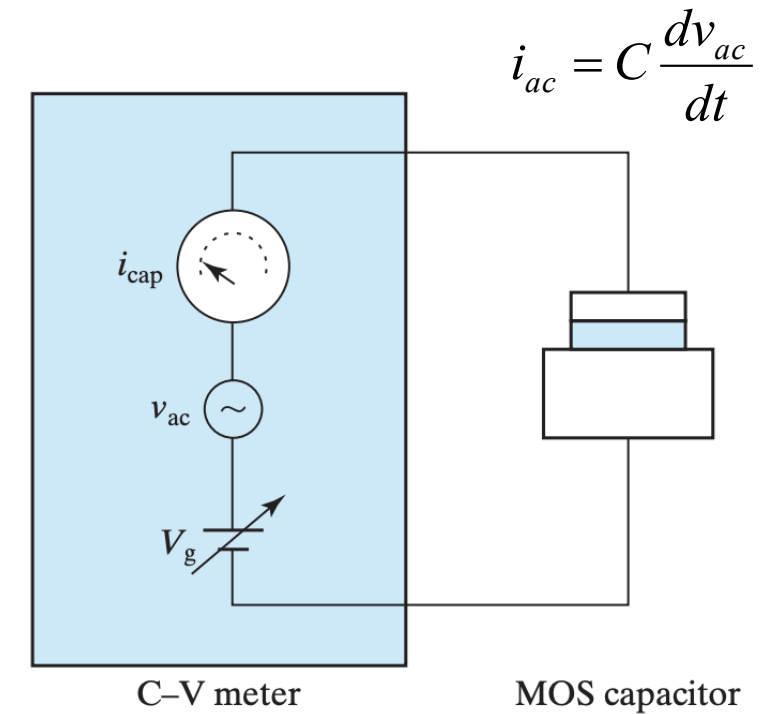
Calculate the flat-band voltage of a silicon NMOS capacitor with substrate doping $N_a = 10^{17} \text{ cm}^{-3}$ and an aluminum gate ($\Phi_M = 4.1 \text{ V}$). Assume there is no fixed charge in the oxide or at the oxide-silicon interface. Calculate the threshold voltage given a 20 nm thick oxide ($\epsilon_{ox} = 3.9\epsilon_0$).

MOS C-V Measurement Setup

- Since this is a capacitor, what does the C-V curve look like?
- C-V characterization is powerful and commonly used
- Useful to determine the oxide _____, _____, _____
- Looking at the small-signal capacitance,

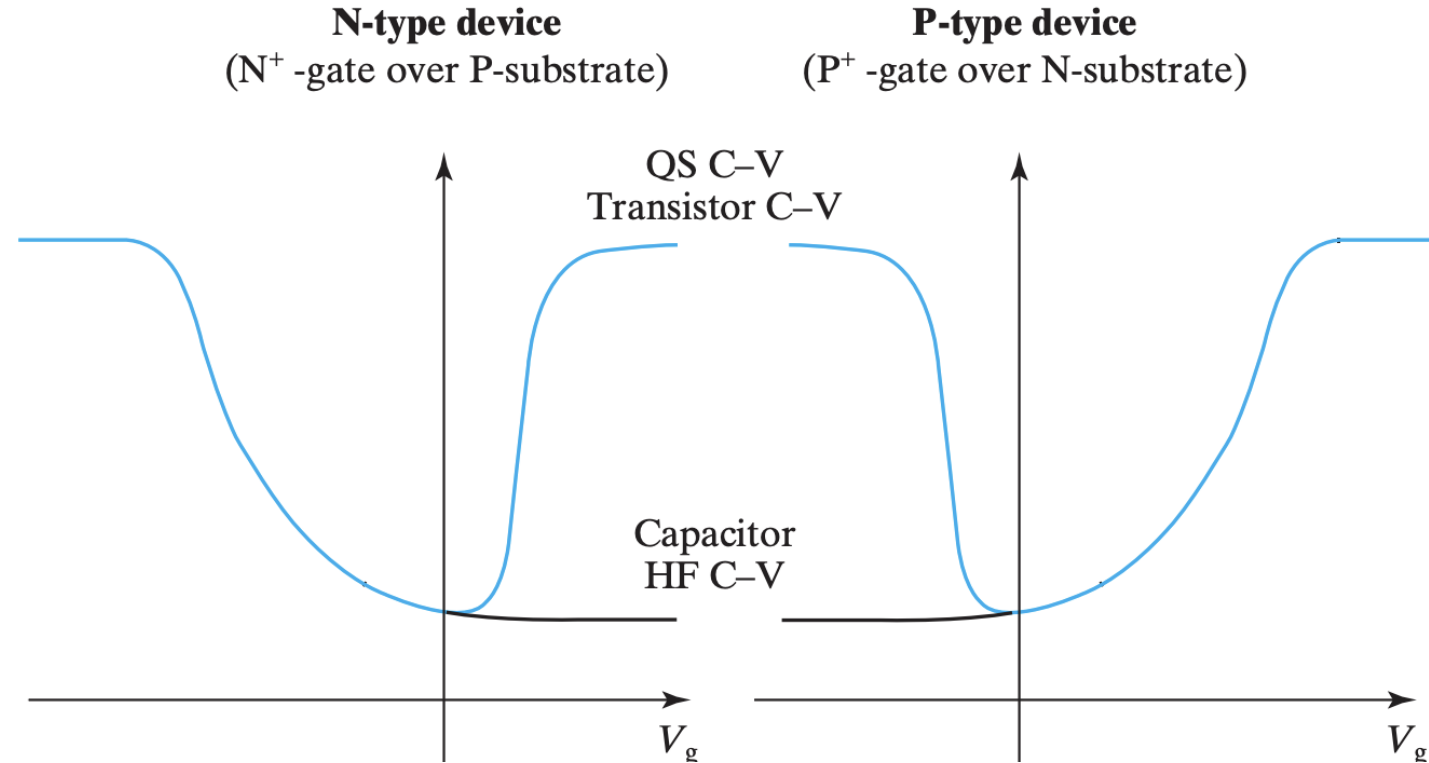
$$C \equiv \frac{dQ_g}{dV_g} = - \frac{dQ_{\text{sub}}}{dV_g}$$

- Recall: (-) sign is because is applied at top plate but is taken at bottom plate
- This C-V curve is idealized
- Question: is the substrate p-type or n-type?
How do we tell?



MOS C-V Measurement Setup

- Recall our gate voltage conditions for different biasing!

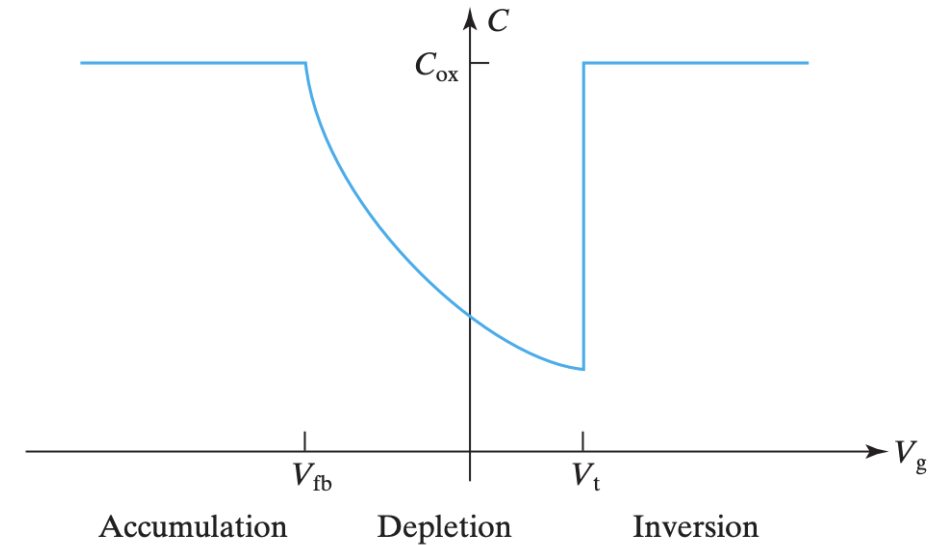


- Which one is PMOS? How about NMOS?

Idealized MOS C-V Curve

- The capacitance is:
$$C_{\text{dep}} = \frac{\epsilon_s}{W_{\text{dep}}}$$
$$\frac{1}{C} = \frac{1}{C_{\text{ox}}} + \frac{1}{C_{\text{dep}}}$$
$$\frac{1}{C} = \sqrt{\frac{1}{C_{\text{ox}}^2} + \frac{2(V_g - V_{\text{fb}})}{qN_a\epsilon_s}}$$
- Where we have solved for W_{dep} in terms of _____ using our earlier relation:

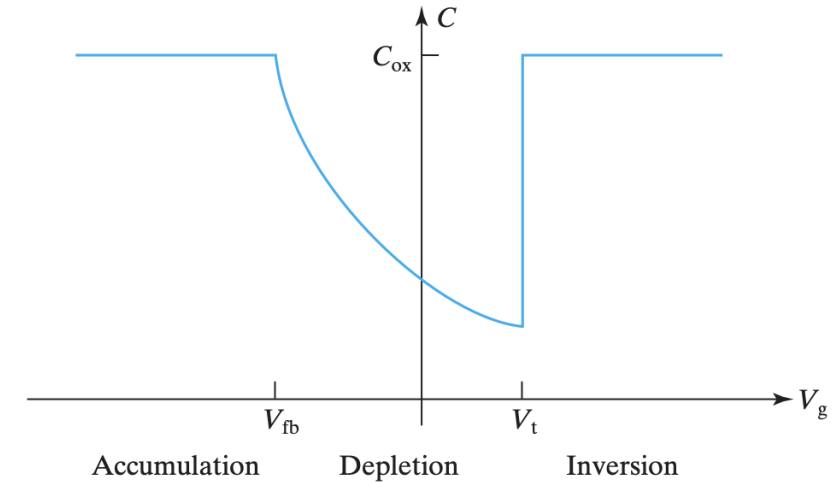
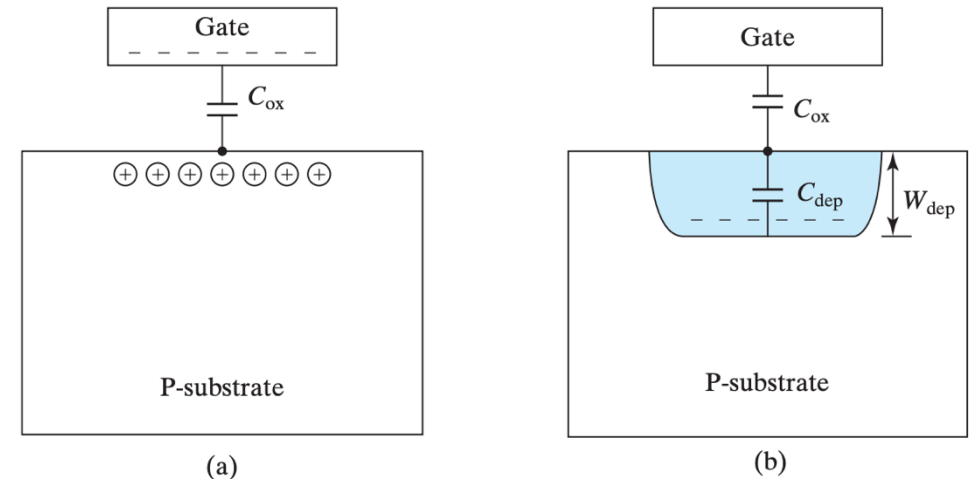
$$V_g = V_{\text{fb}} + \phi_s + V_{\text{ox}} = V_{\text{fb}} + \frac{qN_a W_{\text{dep}}^2}{2\epsilon_s} + \frac{qN_a W_{\text{dep}}}{C_{\text{ox}}}$$



MOS C-V Curve: Accumulation and Depletion

- Let's look at the curve from left to right (increasing ____)
- Accumulation: there is no depletion region so ____ = 0 and $C = C_{ox}$
- Depletion: Our equation above tells us that as V_g increases beyond V_{fb} , W_{dep} ____ and therefore C ____
- But why does $C = C_{ox}$ in the inversion region?

(a) Accumulation region; (b) depletion region



MOS C-V Curve: Inversion Cases

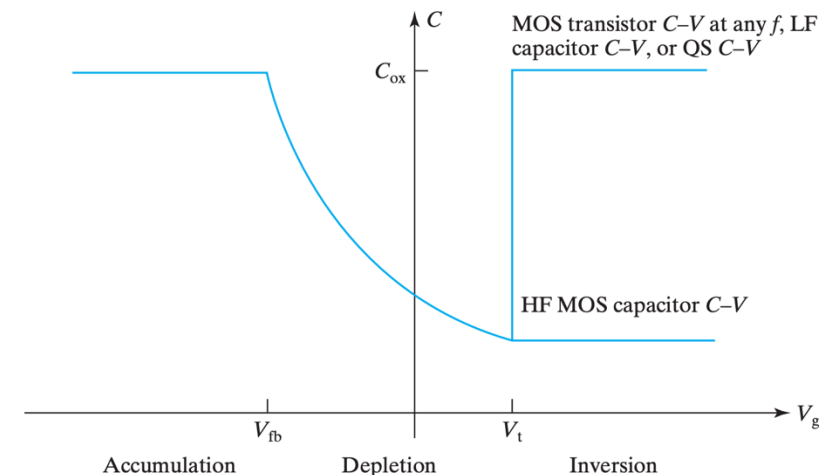
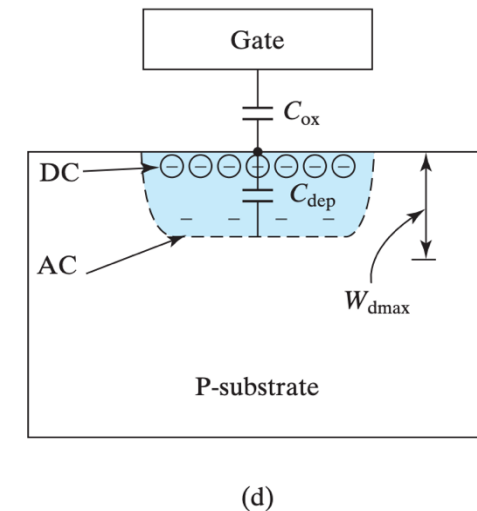
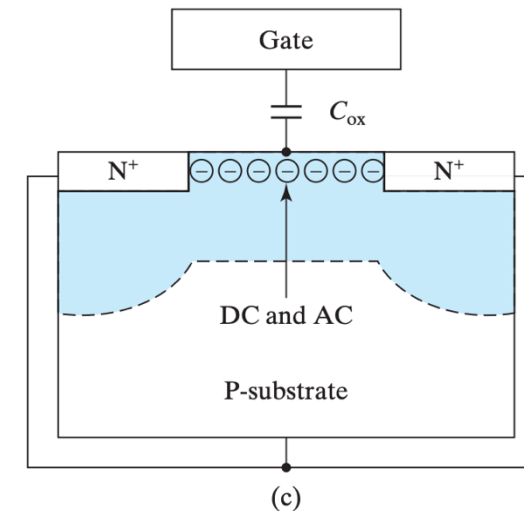
Inversion Case I: inversion layer _____ can be supplied quickly enough to respond to changes in V_g

- Called _____ (QS) C-V
- This case hold true at *low frequencies* (LF)
- How are they supplied?
 1. Optical generation
 2. Providing a nearby source of minority carriers like in a _____

Inversion Case II: inversion layer charge ____ cannot be supplied quickly enough to respond to changes in V_g

- _____ is slow!
- This case hold true at *high frequencies* (HF)
- Q_{inv} cannot respond to fast AC signal and remains constant at DC value
- W_{dep} will expand or contract slightly around _____ (relies on majority carriers). So AC charge exists at the bottom of dep. reg.
- This means our C-V curve looks different depending on the gate voltage frequency: HF, or LF/QS

(c) inversion region with efficient supply of e- from the n+ regions in a MOSFET; (d) inversion region with no or weak supply of inversion e-



C-V of MOS Capacitor vs MOSFET

- What values are considered “high” or “low” frequency?
- Depends on _____!
 - E.g. whether we have an efficient source of _____
- MOSFETs (transistors) remain QS up to _____ frequencies than MOS Caps
- In other words, MOS Caps will enter inversion case II at lower frequencies than MOSFETs

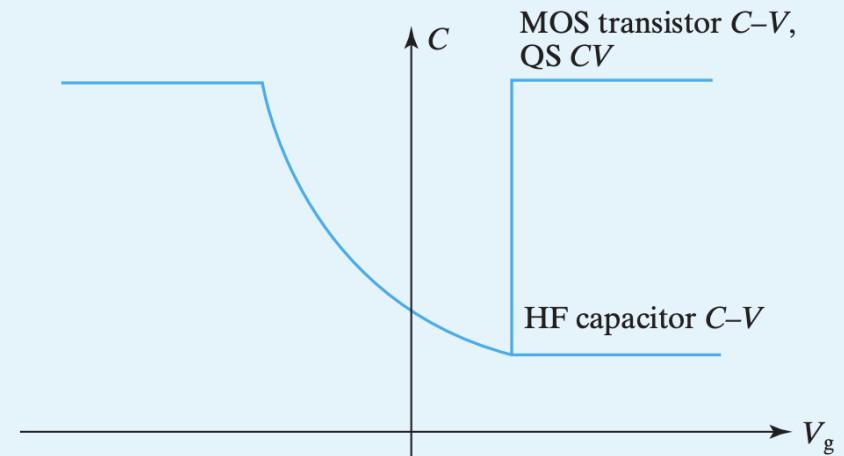


FIGURE 5-19 C-V curves of MOS capacitor and transistor.

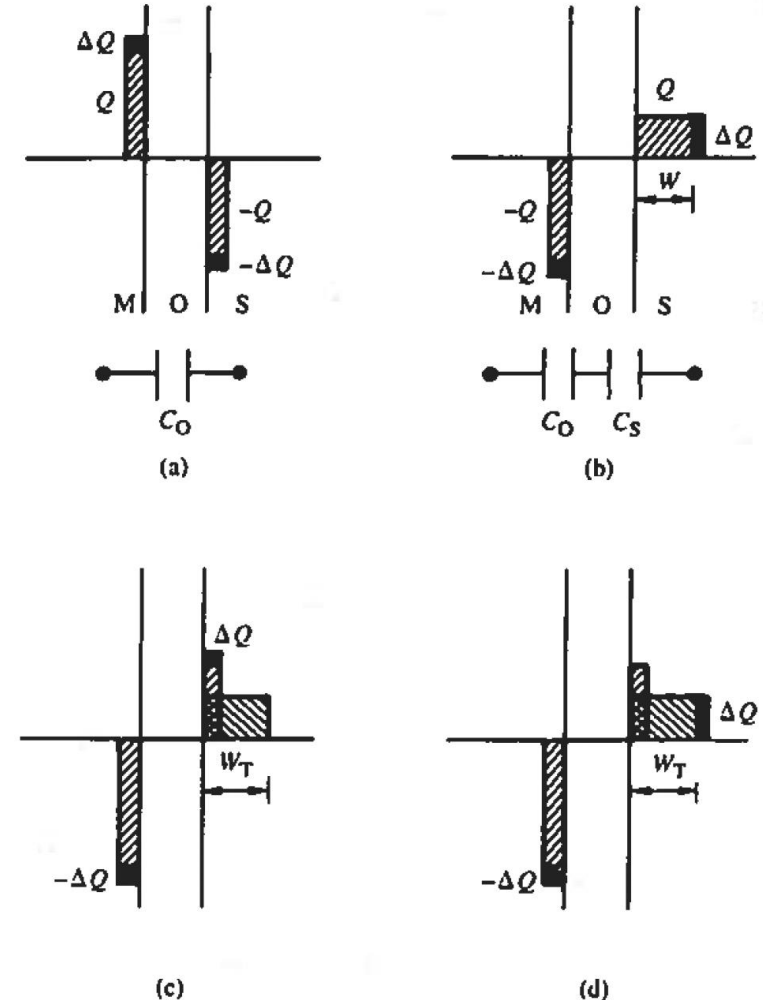
For each of the following cases, does the QS C-V or the HF capacitor C-V apply?

- | | |
|--------------------------------------|-----------------------------|
| (1) MOS transistor, 10 kHz. | (Answer: QS C-V). |
| (2) MOS transistor, 100 MHz. | (Answer: QS C-V). |
| (3) MOS capacitor, 100 MHz. | (Answer: HF capacitor C-V). |
| (4) MOS capacitor, 10 kHz. | (Answer: HF capacitor C-V). |
| (5) MOS capacitor, slow V_g ramp. | (Answer: QS C-V). |
| (6) MOS transistor, slow V_g ramp. | (Answer: QS C-V). |

Charge Fluctuations under AC Conditions

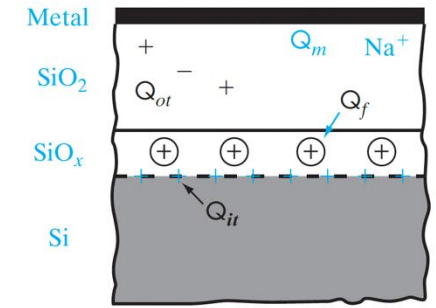
- Note: C_{ox} is the being added or subtracted close to the edges of the insulator
- Black shaded regions represent _____, change in charge from AC signal
- Accumulation: pile-up of e-. _____ driven process! State of system can be changed rapidly
- Depletion: dep. layer charge from withdrawal of majority carriers from W_{dep}
Once again – _____ carrier process! W_{dep} can fluctuate almost instantaneously
- Inversion Case I: Minority carriers are piled up at the interface. As $\omega \rightarrow$ _____, minority carriers _____ be generated or annihilated in response to AC signal
 - Charge is added or subtracted close to _____ in inversion layer.
- Inversion Case II: As $\omega \rightarrow$ _____, sluggish minority carrier R/G processes _____ supply/eliminate minority carriers in response to AC signal
 - # of carriers in inversion layer therefore remains fixed at _____. Depletion region charge fluctuates around $W_{d,max}$
 - Because $W_{d,max}$ is independent of DC V_g , our HF C-V curve is also _____ in inversion case 2 but lower than in case 1 since we have the equivalent of 2 parallel plate caps now

(a) Accumulation, (b) depletion, (c) inversion at low frequency, (d) inversion at high frequency



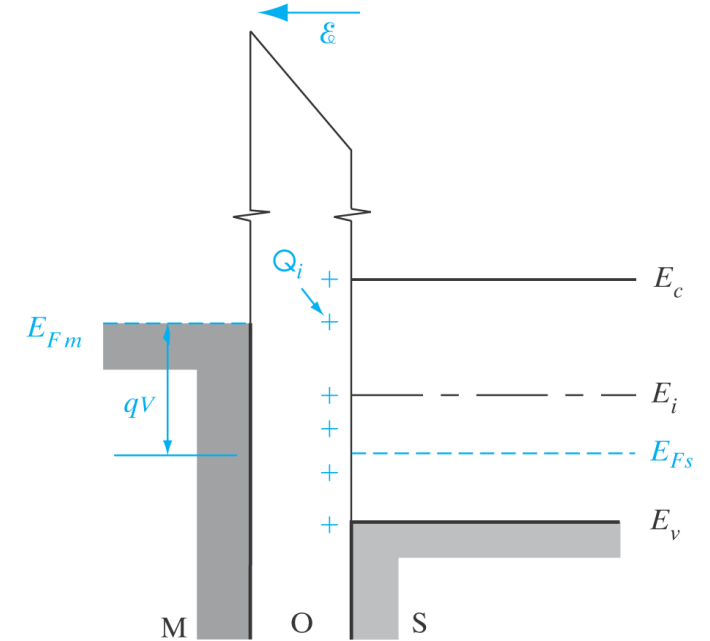
MOS Cap Non-Idealities

- The insulator (dielectric) and O-S interface are not atomically perfect
 - Mobile ions
 - Dangling bonds
 - Charge trapped within _____
- How do we account for these charges?
- We can group them together as an equivalent sheet of charge _____ at the O-S interface
- The (+) charge _____ the E-bands at the interface and changes the field across the insulator!
- This shifts the flat band voltage: $V_{fb} = \Phi_{ms} - Q_i/C_{ox}$
- This interface charge is why $V_g = V_{fb} \neq 0$ in reality!



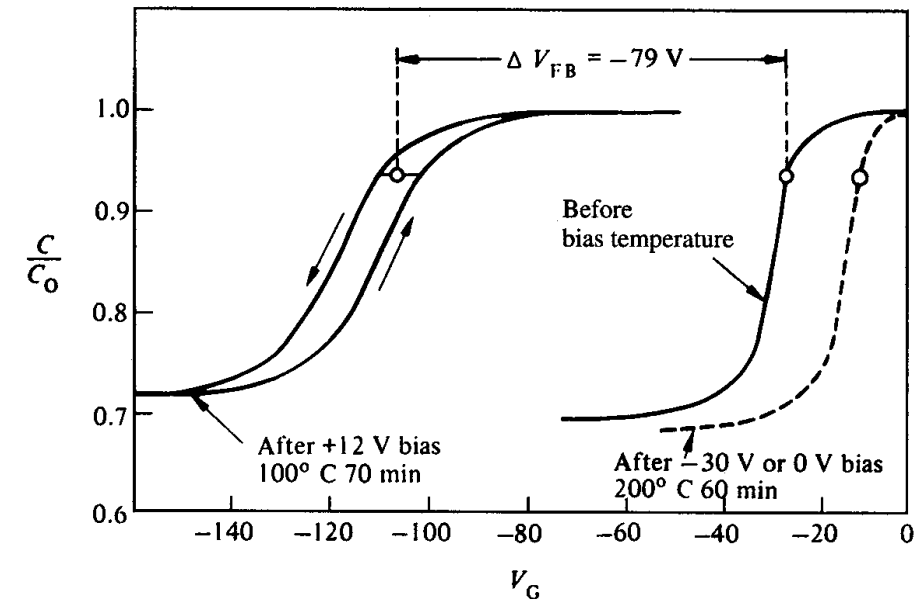
Q_m Mobile ionic charge
 Q_{ot} Oxide trapped charge
 Q_f Oxide fixed charge
 Q_{it} Interface trap charge

(a)



MOS Cap Non-Idealities

- Odd shifts with _____ and _____ in the measured C-V characteristics were once a mystery
- Source of the problem: mobile _____ (e.g. Na⁺, K⁺) moving to/away from interface
 - $\Delta V_{fb} = Q_i / C_{ox}$
- Solution?
- With simple C-V, we can learn and debug a great deal about the properties and quality of MOS caps:
 - Obtain oxide thickness from C in accumulation
 - Obtain substrate doping from C at V_t (HF)
 - Interface charge (Q_i) at V_{fb} from C-V across various oxide thicknesses!



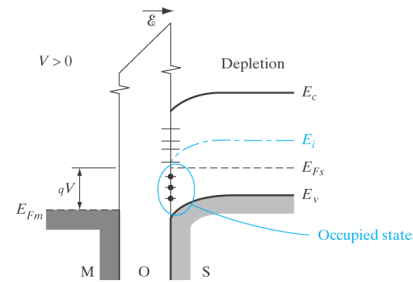
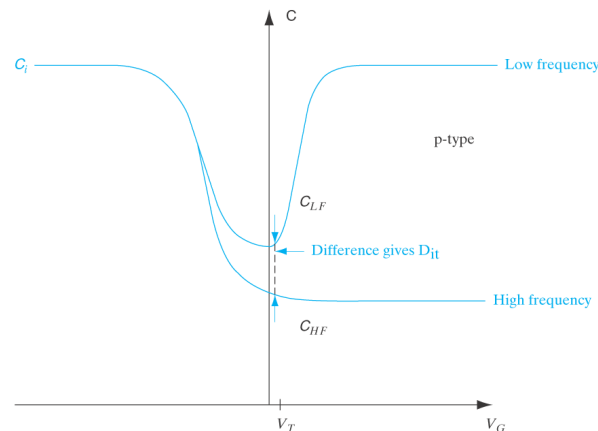
Influence of Material Parameters on Threshold Voltage

- In our ideal case, we found

$$V_t = V_{fb} + 2\phi_B + \frac{\sqrt{qN_a 2\epsilon_s 2\phi_B}}{C_{ox}}$$

- In the non-ideal case, our threshold voltage must be modified to accommodate the ionic charge

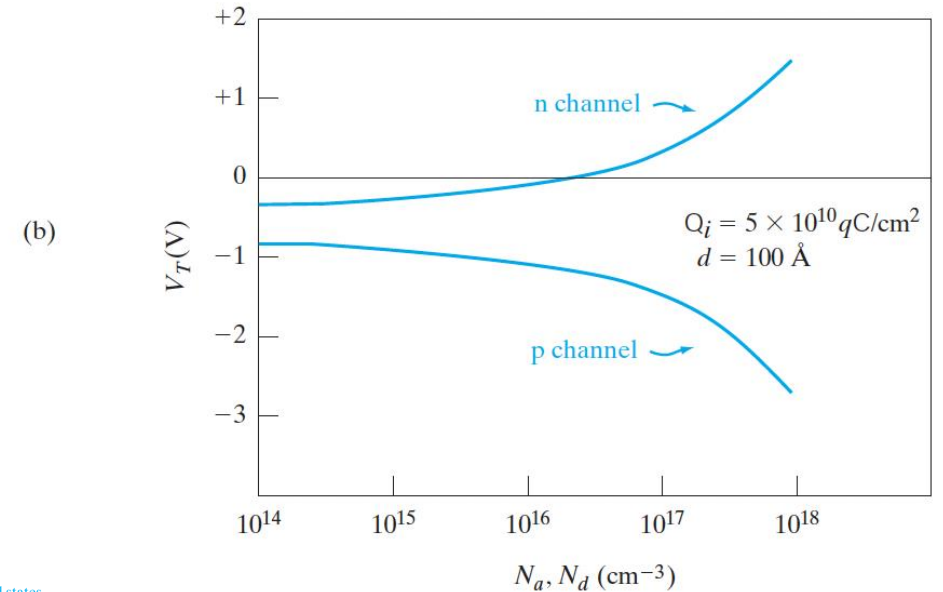
(traps): $V_t = \Phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_{dep}}{C_{ox}} + 2\Phi_F$



$$\Phi_{ms} = \Phi_m - \Phi_s$$

(a)

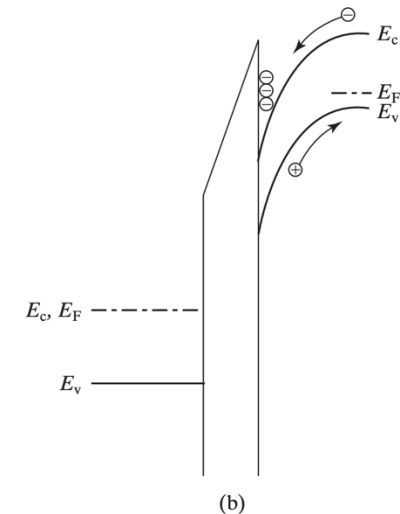
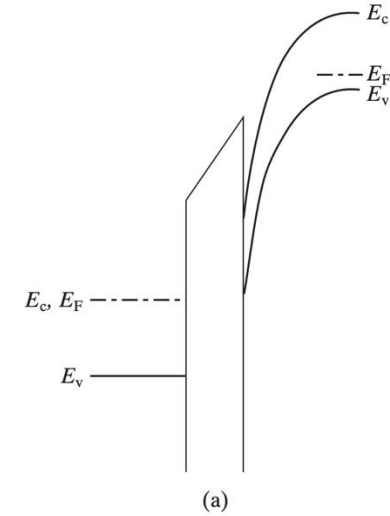
| | | | | |
|---------|-------------|--------------------|--------------------------------|--------------------------------|
| $V_T =$ | Φ_{ms} | $-\frac{Q_i}{C_i}$ | $-\frac{Q_d}{C_i}$ | $+2\Phi_F$ |
| | (-) | (-) | (+) n channel (-) p channel | (+) n channel (-) p channel |



Application: CCD Imager

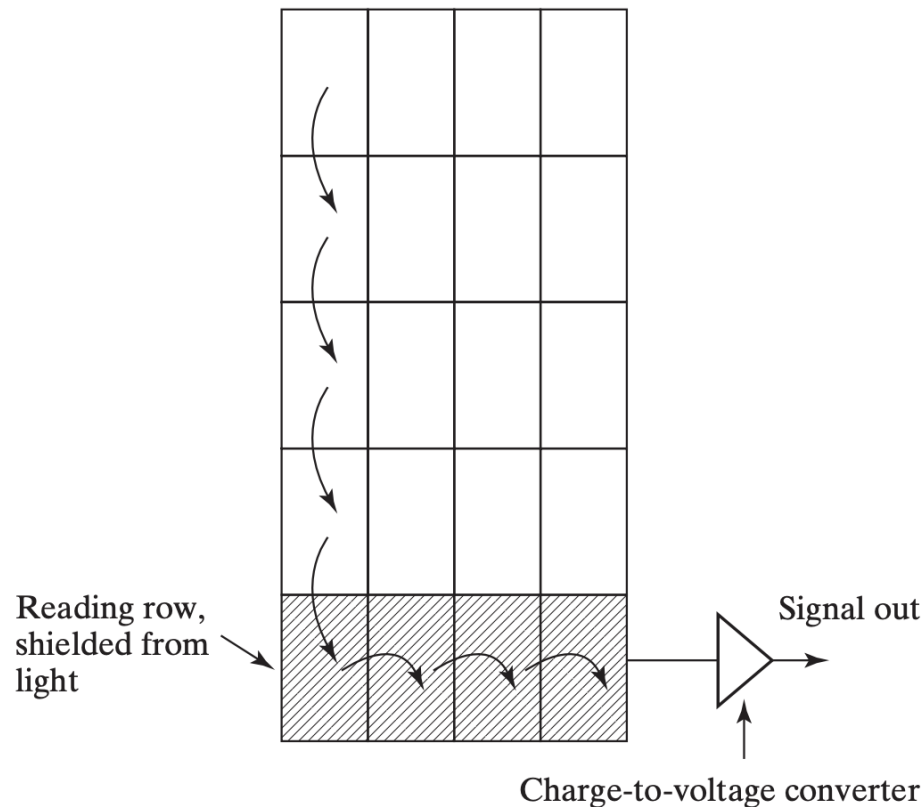
- MOS caps rarely used stand alone *except* for _____
- _____! Imager = sensing device that converts optical image into _____
- Large # of MOS caps are packed into a 2D _____
- nMOS: Immediately after we apply $V_g > V_t$, there are no e- on surface yet (no _____). Thermal generation is slow!
- The bands bend beyond $2\Phi_B$ and W_d _____ $W_{d,max}$ for a fraction of a second. This is called _____.
- If light shines on the MOS cap for these tens of ms, # of photo-generated e- collected at interface is proportional to _____.
- We have now converted an image (2D pattern of light intensity) into packets of e- stored in a 2D array of MOS caps!

Deep depletion (a) immediately after $V_g > V_t$ applied, no e- at surface yet. (b) After exposure to light, photo-generated e- collect at surface.



Application: CCD Imager

- How do we transfer these collected "charge packets" to the edge of the array so they can be read into charge sensing _____?



Portion of a row in array is biased in the sequence (a), (b), (c), etc. The charge packets in (c) are shifted to the right by one capacitor compared to (a)

